REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the following remarks.

The Applicants originally submitted Claims 1-20 in the application. In a previous response to an Election Requirement, the Applicants elected Claims 1-10 and 16-20 (representing Group II) and withdrew Claims 11-15. Presently, the Applicants have not amended, canceled nor added any claims. Accordingly, Claims 1-10 and 16-20 are currently pending in the application.

I. Rejection of Claims 1-3, 9-10, 16 and 20 under 35 U.S.C. §103

The Examiner has rejected Claims 1-3, 9-10, 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,528,327 to Nagano, *et al.* ("Nag") in view of U.S. Patent No. 6,277,731 to Gonzalez, *et al.* ("Gonzalez"). Independent Claims 1 and 16 currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean.

Nag is directed to a method for fabricating semiconductor device memory having a capacitor. (Title). Nag teaches that a conductive layer **17** located within a contact hole **16** in and over an upper surface of a passivation film **15** is polished to remove the entire conductive layer **17** from an upper surface of the passivation film **15**. Nag specifically teaches that the conductive layer **17** is over

polished for a period of time about 20% to 30% longer than normally required to remove all residue on an upper surface of the passivation film **15**. This over polish not only removes the entire conductive layer **17** from the upper surface of the passivation film **15**, but also creates a recess in the passivation film **15**.

Gonzalez is directed to a method for forming a semiconductor connection with a top surface having an enlarged recess. (Title). Gonzalez teaches that a top surface of an interconnect may be subjected to a cleaning step after being subjected to a CMP step. Gonzalez teaches that the surface of the integrated circuit **10** is cleaned, for example, by a bath of hydrofluoric acid that cleans the surface **16** of the dielectric layer **2** and opens up a small recess **30** in the glue and barrier layers **22** and **24** around the edge **29** of the plug **26**. (Column 5, lines 7-20 of Gonzalez).

The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the post-planarization clean of Gonzalez in the method of forming an interconnect of Nag. The Examiner further asserts that one would have been motivated to do this because performing a post-planarization clean was a conventional method of removing residue left from a CMP step from the surface of a layer to prevent latent defects in the integrated circuit and improve device performance. The Applicants respectfully disagree with the Examiner.

No motivation exists in either of Nag or Gonzalez to combine the post-planarization clean of Gonzalez with the method of forming the interconnect of Nag. Nag, without any teachings of Gonzalez, addresses the removal of the residue in its own manner. Specifically, Nag requires that the conductive film **17** and the passivation film **15** be overpolished for a period of time about 20% to 30% longer than normally to remove all residue on an upper surface of the passivation film **15**. After

conducting the overpolishing of the conductive film 17 and the passivation film 15 as taught by Nag, no residue would remain for the post-planarization clean to remove. As the industry desires removing unnecessary steps, and not adding unnecessary steps, one skilled in the art would not be motivated to follow the overpolishing of the conductive film 17 and the passivation film 15 with the post-planarization clean, as the Examiner asserts.

There is also no motivation to replace the overpolishing of the conductive film 17 and the passivation film 15 as taught by Nag, with the post-planarization clean as taught by Gonzalez. Namely, no motivation exists to swap these teaching because the teachings of Nag would be frustrated. Accordingly, the only person that would be motivated to follow the overpolishing of the conductive film 17 and the passivation film 15 with the post-planarization clean, or alternatively replace the overpolishing of the conductive film 17 and the passivation film 15 as taught by Nag with the post-planarization clean as taught by Gonzalez, would be a person using the present invention as a blueprint to reconstruct the claimed invention. The Examiner is well aware that such a combination is improper.

Therefore, there is no motivation in Nag or Gonzalez to combine their teachings. As each of Nag and Gonzalez fails to teach or suggest at least one claimed element of independent Claims 1 and 16, the references fail to establish a prima facie case of obviousness with respect to these claims, and any claims that may depend therefrom. Claims 1-3, 9-10, 16 and 20 are therefore not obvious in view of Nag and Gonzalez.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1-3, 9-10, 16 and 20 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

II. Rejection of Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103

The Examiner has rejected Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103(a) as being unpatentable over Nag in view of Gonzalez and as described above, and further in view of U.S. Pub. No. 2005/0148190A1 to Dubin, *et al.* ("Dubin"). Independent Claims 1 and 16 currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean. As previously established, the combination of Nag and Gonzalez is improper. As also previously established, Nag and Gonzalez alone fail to teach or suggest these elements.

Dubin further fails to teach or suggest these elements. The Examiner is offering Dubin for the sole proposition of the process conditions that might be used to remove a recess. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of the process conditions that might be used to remove a recess is entirely different from a teaching or suggestion of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean, as currently claimed. Accordingly, Dubin also fails to teach or suggest these claimed elements.

Thus, Nag or Gonzalez, individually or in combination with Dubin, fail to teach or suggest the invention recited in independent Claims 1 and 16 and their dependent claims, when considered as a whole. The combination therefore fails to establish a prima facie case of obviousness with respect to these claims. Claims 4, 6-7, 17 and 19 are therefore not obvious in view of Nag, Gonzalez and Dubin.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

III. Rejection of Claims 5, 8 and 18 under 35 U.S.C. §103

The Examiner has rejected Claims 5, 8 and 18 under 35 U.S.C. §103(a) as being unpatentable over Nag in view of Gonzalez and Dubin, and further in view of U.S. Patent No. 6,313,003 to Chen ("Chen"). As previously mentioned, independent Claims 1 and 16 currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean. As previously established, the combination of Nag, Gonzalez and Dublin is either improper or fails to teach or suggest these claimed elements.

Chen further fails to teach or suggest these elements. The Examiner is offering Chen for the sole proposition of the process conditions that might be used to remove a recess. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of the process conditions that might be used to remove a recess is entirely different from a teaching or suggestion of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean, as currently claimed. Accordingly, Chen also fails to teach or suggest these claimed elements.

Thus, Nag or Gonzalez, individually or in combination with Dubin and/or Chen, fails to teach or suggest the invention recited in independent Claims 1 and 16 and their dependent claims,

when considered as a whole. The combination therefore fails to establish a prima facie case of obviousness with respect to these claims. Claims 5, 8 and 18 are therefore not obvious in view of Nag, Gonzalez, Dubin and Chen.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 5, 8 and 18 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

IV. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-10 and 16-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 20-0668.

Respectfully submitted,

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